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THE PULSE-POSITION-MODULATION TELEMETRY VIDEO MONITOR

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GSFC

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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July 1969

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ABSTRACT

The Video Monitor is part of the Pulse-Position-Modulation Telemetry ground station of the Sounding Rocket Branch of Goddard Space Flight Center. It is used to display certain waveforms that are useful in adjusting the station equipment. It is so designed and so connected to the station equipment that, by the turning of one control, the operator is able to select a particular waveform, the portion of it to be viewed, and the best sweep length for displaying it.

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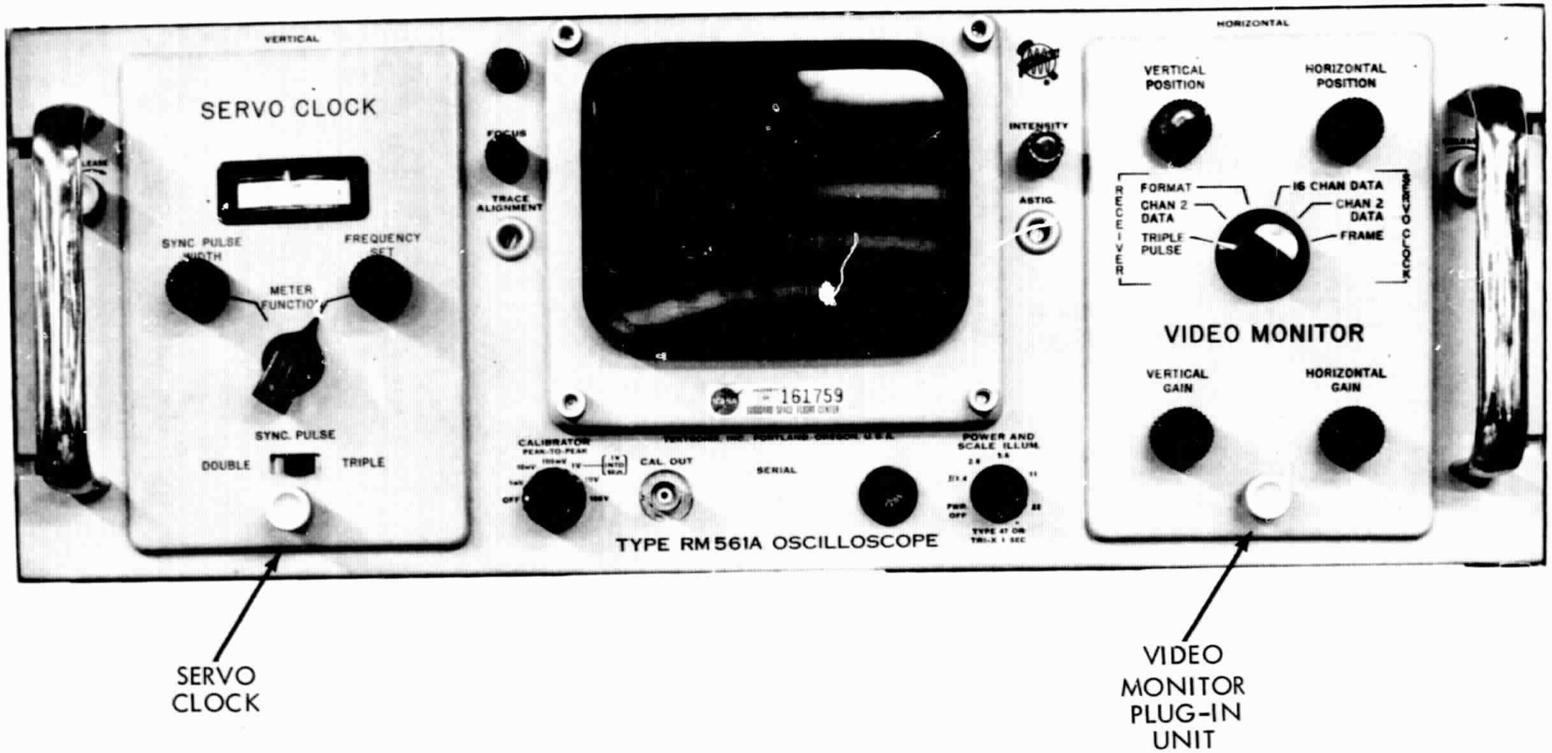

Frontispiece — Video Monitor, Showing the Servo Clock Plug-In Unit

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THE PULSE-POSITION-MODULATION TELEMETRY VIDEO MONITOR

INTRODUCTION

The Pulse-Position-Modulation (PPM) Ground Station's Video Monitor is a special oscilloscope whose purpose is to display certain waveforms as an aid in adjusting the station for operation.

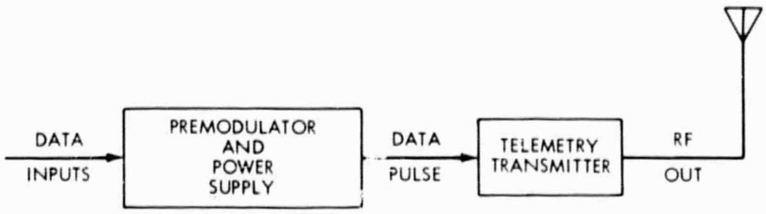
PULSE-POSITION-MODULATION SYSTEM

A complete PPM telemetry system consists of one or more telemeters, or vehicle-borne encoder-transmitters, and a ground station, which receives and records the telemetry signals. (See Figure 1.)

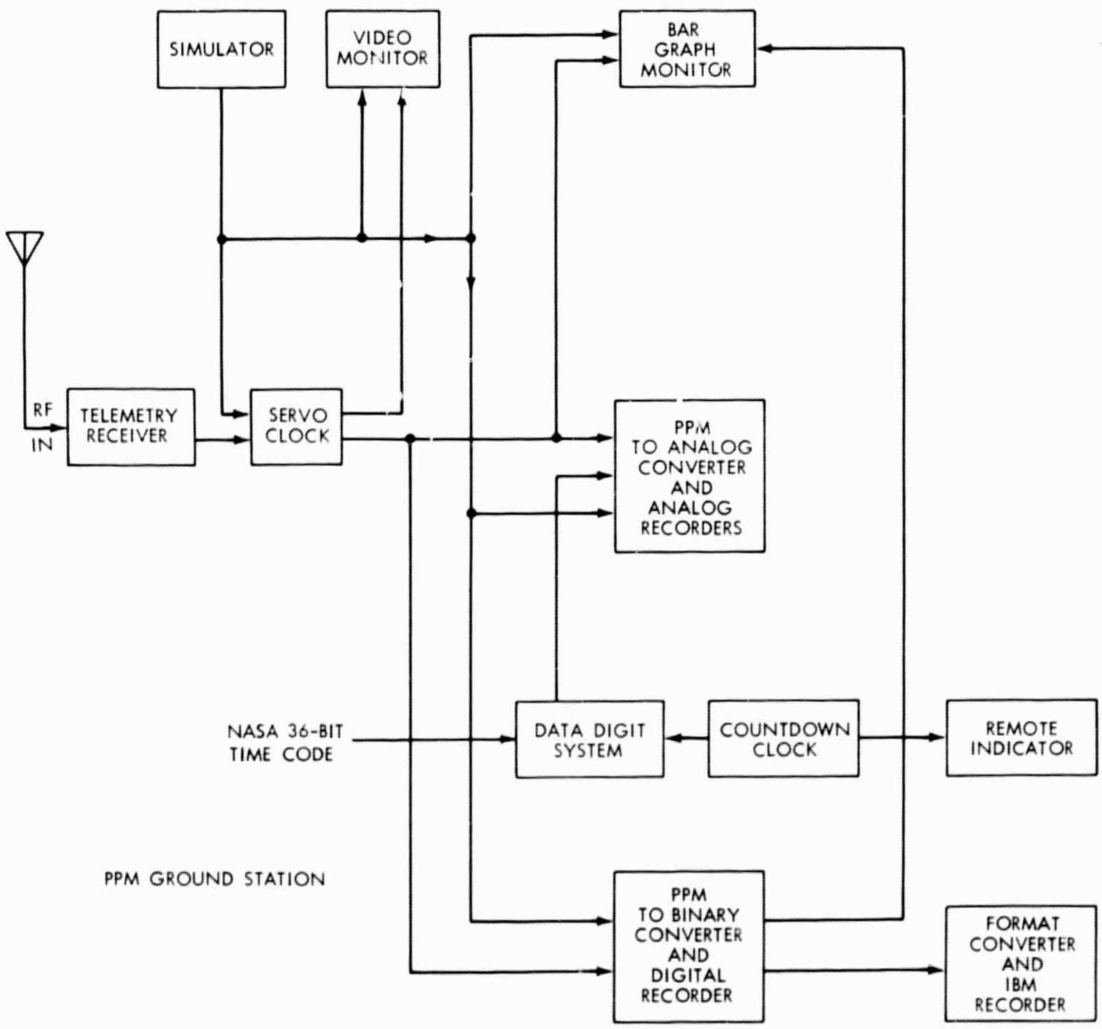
The PPM telemetry system used by the Sounding Rocket Instrumentations Section of Goddard Space Flight Center is a time-sharing multiplex system in which a pulse-position/amplitude-modulation (PPM/AM) system is employed. In this system, the transmitter output is pulse-modulated radio frequency, with full amplitude for a pulse, and zero amplitude in the absence of a pulse. Each of sixteen channels is supplied with data in the form of a voltage in the zero-to-five volts range. Each channel in turn is gated ON, and a pulse is generated. The timing of the pulse, relative to the total ON time for that channel, is a linear function of the input voltage.

The system output consists of a three-microsecond data pulse for each channel, plus a triple pulse at the beginning of CHANNEL 1. The total time reserved for each channel is the reciprocal of the clock rate. The total frame time is sixteen times the time for each channel.

TELEMETER. An unusual part of the Telemeter is the PPM encoder. This contains: a five kilohertz clock; a four-stage counter and a matrix connected to 16 gates; a sawtooth generator, operating at the clock frequency and connected to all the gates; and a pulse generator. The counter-matrix combination ENABLES each gate, in turn. At the time that the sawtooth voltage is equal to the data input voltage, a gate output, which triggers the pulse generator, is produced. An output of the last counter stage triggers the triple pulse generator at the beginning of Channel 1.



SST-3 TELEMETER



PPM GROUND STATION

Figure 1. PPM Telemetry System, Functional Block Diagram

GROUND STATION. The ground station is capable of decommutating the PPM signal, that is, of separating it by channels. This capability is made possible by the Servo Clock, which is slaved to the clock in the transmitter, and which times the channel gates. This clock contains a voltage controlled oscillator whose output frequency is nominally 40 kilohertz, and a frequency divider to provide the clock frequency. The clock output is connected to a one-shot multivibrator to provide the channel reference pulses. This output is divided by a sixteen-to-one counter whose output is fed to another one-shot multivibrator which generates the frame-reference pulse. A phase comparator is used to compare the timing of the frame-reference pulse with that of a pulse derived from the received triple pulse. Any timing difference produces an output voltage, whose magnitude and polarity causes the output frequency of the voltage-controlled oscillator to change. Thus the frame reference-pulse and the triple pulse from the received signal will be locked together in the correct phase relationship. Data pulses and channel reference pulses from the servo clock are fed to PPM-to-binary, and PPM-to-analog, converters for conversion into one or both of these conventional forms in which data are stored.

FUNCTION OF THE VIDEO MONITOR

The Video Monitor is permanently connected, both to the output of the telemetry receiver, and to the output of the Video Clock. By merely rotating a front-panel control, the station operator can select either of these outputs to be displayed, as a whole, or in selected parts, on the screen of the Cathode-ray tube.

PHYSICAL DESCRIPTION

The Video Monitor consists of a Tektronix Model RM 561A oscilloscope, on which certain modifications have been made. Mechanically, the only changes consist of removing the horizontal and vertical plug-in units, and the substitution of the special Video Monitor plug-in unit within the space formerly occupied by the horizontal unit. The space originally designed to receive the vertical plug-in unit is, instead, used to house the Servo Clock - another component of the PPM Ground Station - and to provide power and signal connections to it.

MAIN CHASSIS

The basic oscilloscope is the main chassis. It is 19 inches wide 7 inches high and 18 inches from front to back. It is completely enclosed, having top and bottom cover plates that are perforated for ventilation, and it contains a forced-ventilation fan. It is mounted in the rack on drawer-type slides.

PLUG-IN UNIT

The plug-in unit containing most of the special circuitry is mechanically interchangeable with either the horizontal or the vertical plug-in unit of the oscilloscope. This unit is 6 inches high by 4 inches wide by 12 inches deep. It has connectors, and guide rails for two printed wiring cards. On the rear of the unit is mounted a connector, which mates with the oscilloscope wiring connector. Figures 2 and 3 show top and bottom views, respectively, of this unit.

PRINTED-WIRING CARDS

The printed-wiring cards (Figure 4), approximately 4-1/8 inches by 4-3/8 inches in size, consist of laminated board on which all the wiring and connector pins have been etched. A lever is provided on one corner of each card to facilitate disengagement of the board from the connector.

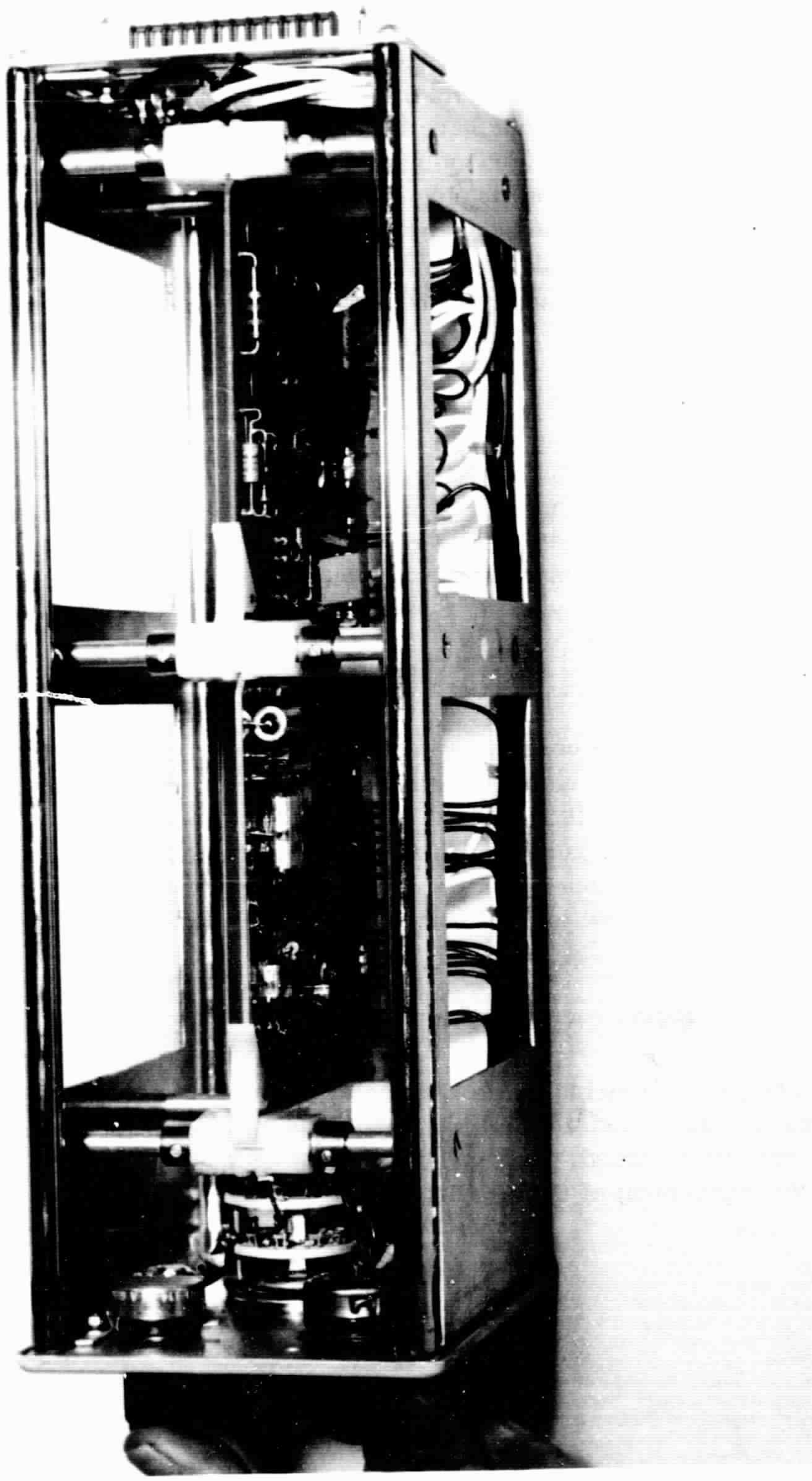


Figure 2. Plug-In Unit, Top View

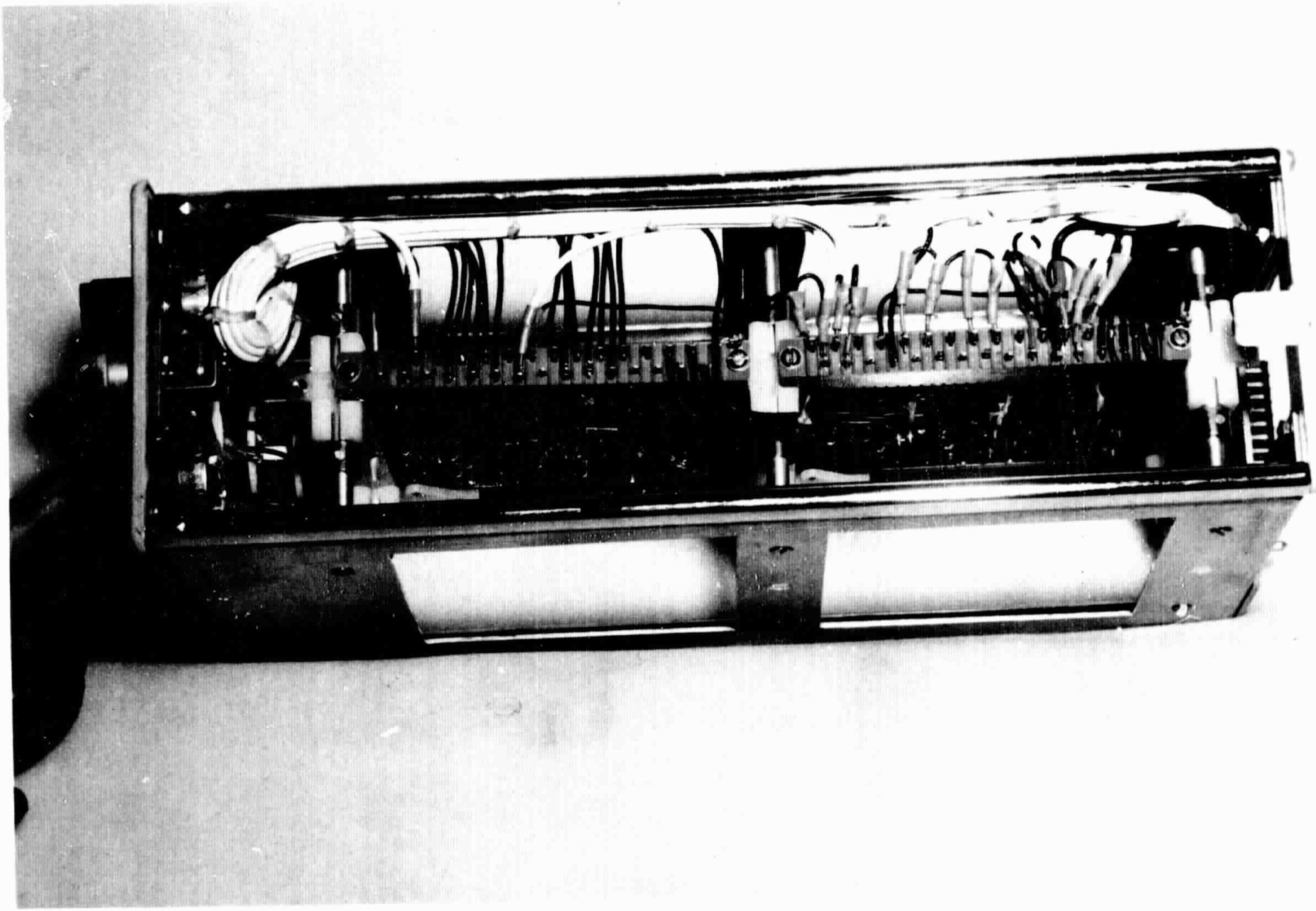
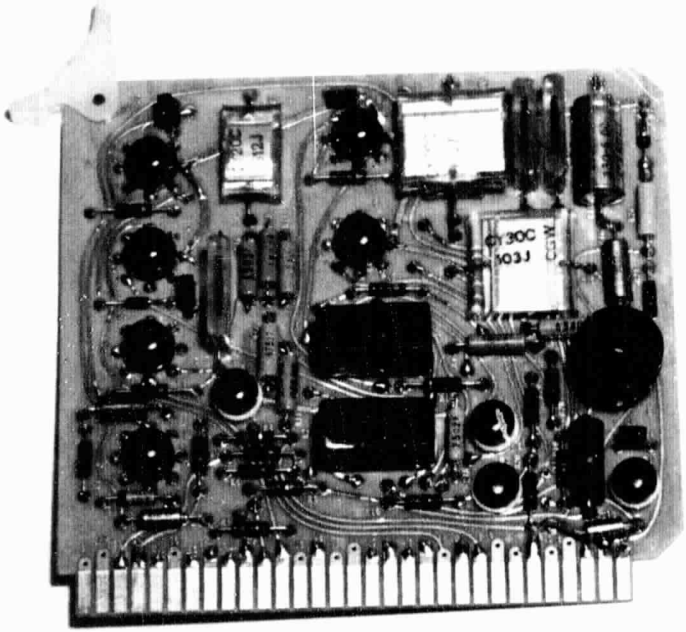
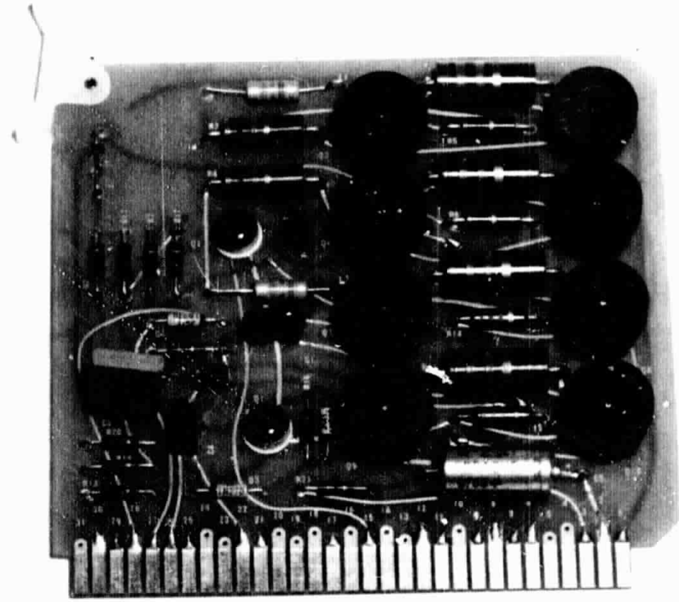


Figure 3. Plug-In Unit, Bottom View



Video Monitor Card 1



High-Level Amplifier Card

Figure 4. Printed Wiring Card, Assemblies

CAPABILITY

The Video Monitor is permanently connected to the circuits containing the waveforms to be monitored, and to the outputs of the pulses to be used as synchronizing pulses. The only adjustment required to view any specified waveform is to turn a front-panel control to the position of that designation.

INPUTS

The Video Monitor requires, as inputs: the FORMAT output of the receiver; plus the DATA, FRAME, CHANNEL TWO, and CHANNEL 16 (ONE-HALF pulse) outputs from the Servo Clock.

RECEIVER FORMAT OUTPUT. The output of the telemetry receiver, when receiving the PPM telemetry signal, is called the FORMAT. This consists of a continuous train of a single TRIPLE PULSE, followed by sixteen DATA pulses.

SERVO CLOCK, DATA OUTPUT. The DATA output of the Servo Clock consists only of DATA pulses, as opposed to the FORMAT output, which contains a TRIPLE PULSE for each sixteen DATA pulses.

FRAME PULSE. The FRAME pulse is a 4-microsecond 10-volt negative pulse whose beginning coincides with the start of operation of Channel 1, of the 16-channel frame. It may be displayed on the Video Monitor, and it is also used as a synchronizing pulse in triggering the sweep for cetain displays.

CHANNEL-TWO PULSE. The Channel 2 pulse occurs during the time allotted to the Channel 2 functions. It is a positive 3-volt pulse, having the same duration as that of Channel 2 operation, for whatever Clock rate is in use at the time. It is used as a synchronizing pulse.

CHANNEL SIXTEEN, ONE-HALF PULSE. The Channel 16 (one-half) pulse coincides, in time, with the first half of the duration of Channel 16, and has an amplitude of +3 volts. This pulse is also used for synchronization.

DISPLAYS

The Video Monitor is able to display, on the screen of the cathode-ray tube, any one of the following described waveforms, each on a time base of suitable duration for good viewing.

RECEIVER, FORMAT DISPLAY. All of the RECEIVER FORMAT output, except the first 15 microseconds of Channel 1 operation, is displayed with this setting.

RECEIVER, CHANNEL-TWO DATA DISPLAY. When the monitor is set for RECEIVER, CHANNEL-2 DATA, Channel 2 of the RECEIVER FORMAT is displayed on a time base that spreads the CHANNEL-2 DATA waveforms over the entire usable width of the cathode-ray tube.

RECEIVER, TRIPLE-PULSE DISPLAY. The TRIPLE PULSE consists of three 4-microsecond, 10-volt pulses, having a total duration of 20 microseconds. When the Clock rate is 5 kilohertz, the TRIPLE PULSE begins at the same time as Channel 1. At 10- or 20-kilohertz Clock rate, the TRIPLE PULSE begins 25 microseconds after the start of Channel-1 operation. In either case, it can be displayed on a 40-microsecond time base (sweep length).

SERVO CLOCK, SIXTEEN-CHANNEL-DATA DISPLAY. The sixteen channels of the SERVO-CLOCK DATA output are displayed, beginning with Channel 1. On the cathode ray tube, the display begins 15 microseconds after the beginning of Channel 1 operation.

SERVO CLOCK, CHANNEL-TWO-DATA DISPLAY. The Servo Clock CHANNEL-2-DATA display is similar to the Receiver Channel 2 Data display.

FRAME PULSE, DISPLAY. The FRAME pulse is displayed in the same format as is the TRIPLE PULSE, when the latter is displayed during operation at the 5-kilohertz clock rate.

THEORY OF OPERATION

Figures 5 through 8, and A-1 through A-6 in the Appendix, may be used for reference to supplement the explanations given in this section.

SWEEP GENERATOR

The description of the sweep generator can be broken down into three parts: the charging circuitry; the discharge circuitry; and the buffer-feed-back circuitry. Figure 5 contains block diagrams and waveforms for a simple sweep generator and for the sweep generator as used in the Video Monitor.

CHARGING CIRCUITRY. When a capacitor is charged through a resistor, the voltage across the capacitor rises at a rate that is proportional to the current. If a constant current is used to charge the network, the voltage rise is linear. This voltage, when amplified and applied to the two horizontal deflection plates of the cathode-ray tube, drives the trace horizontally across the screen at a uniform rate. When charging with a constant-voltage, the voltage across the capacitor will subtract from the total voltage, and the voltage across the resistor will become progressively less, as the capacitor becomes charged. The result is that the charging takes place at an exponential rate rather than a linear rate. This effect is overcome in the Video Monitor by the type of feedback used, which will be described in the section on "Buffer-Feedback Circuitry." (See Page 16.)

At each position of the selector switch, a different resistor or combination of resistors is connected between the capacitor and the 7.5-volt zener-diode regulated power source. In each case, a resistance value is chosen that will permit the capacitors to charge up to approximately +8 volts during the sweep time. Where the sweep length is also a function of the clock rate, as is the situation with the CHANNEL 2 DATA, the FORMAT, and the 16-CHANNEL DATA, the resistor values are also changed by relays.

DISCHARGE CIRCUITRY. A transistor is connected in parallel with the capacitor having its collector connected to the charging resistor network, and its emitter connected to ground. Its base is connected to the selector switch section that selects the different timing waveforms. A low level (0 volt) on the base of the transistor causes its impedance to be very high, and allows the capacitor to be charged in a linear manner. A HIGH level (+3.6 volts) on its base causes the impedance of the transistor to be very low; and the capacitor discharges through the transistor. The period during which the LOW voltage appears at the discharge transistor base is called the SWEEP GATE.

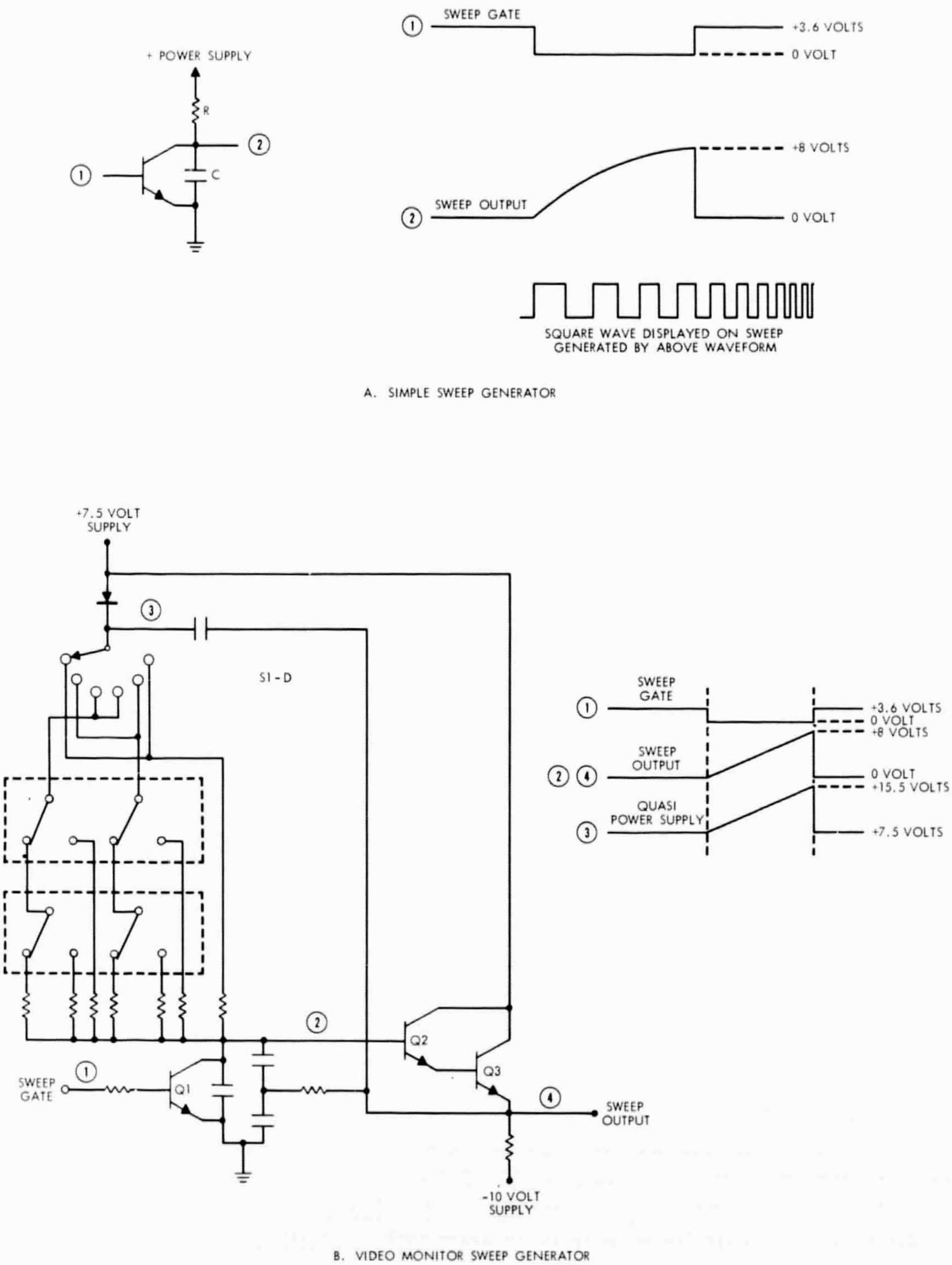


Figure 5. Sweep Generator, Schematic Diagram and Waveforms

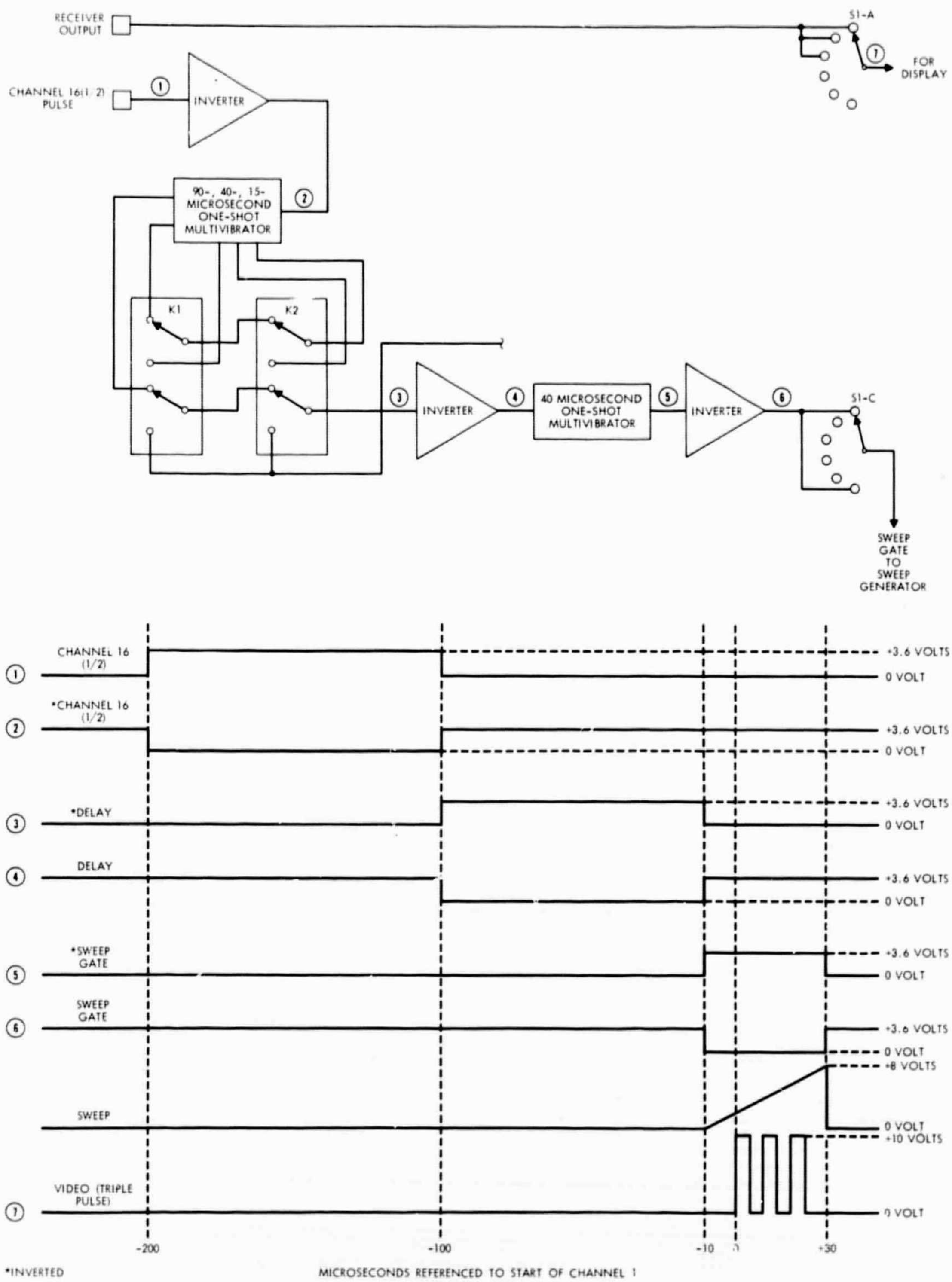


Figure 6. Sweep-Gate Pulse Generation, Diagram and Waveforms for Triple Pulse Display (5-Kilohertz Clock Rate)

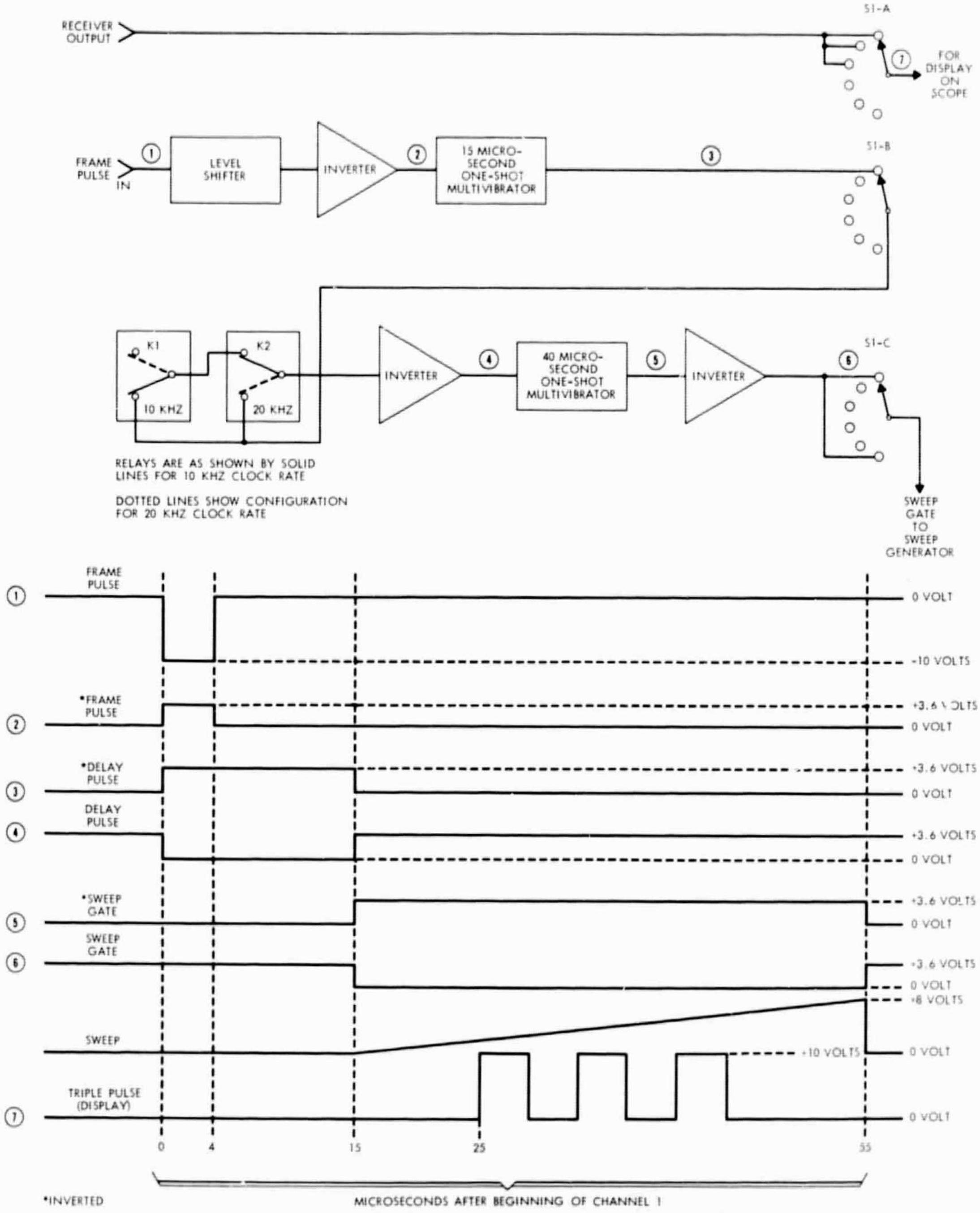


Figure 7. Sweep-Gate Pulse Generation, Diagram and Waveforms for Triple Pulse Display (10- and 20-Kilohertz Clock Rates)

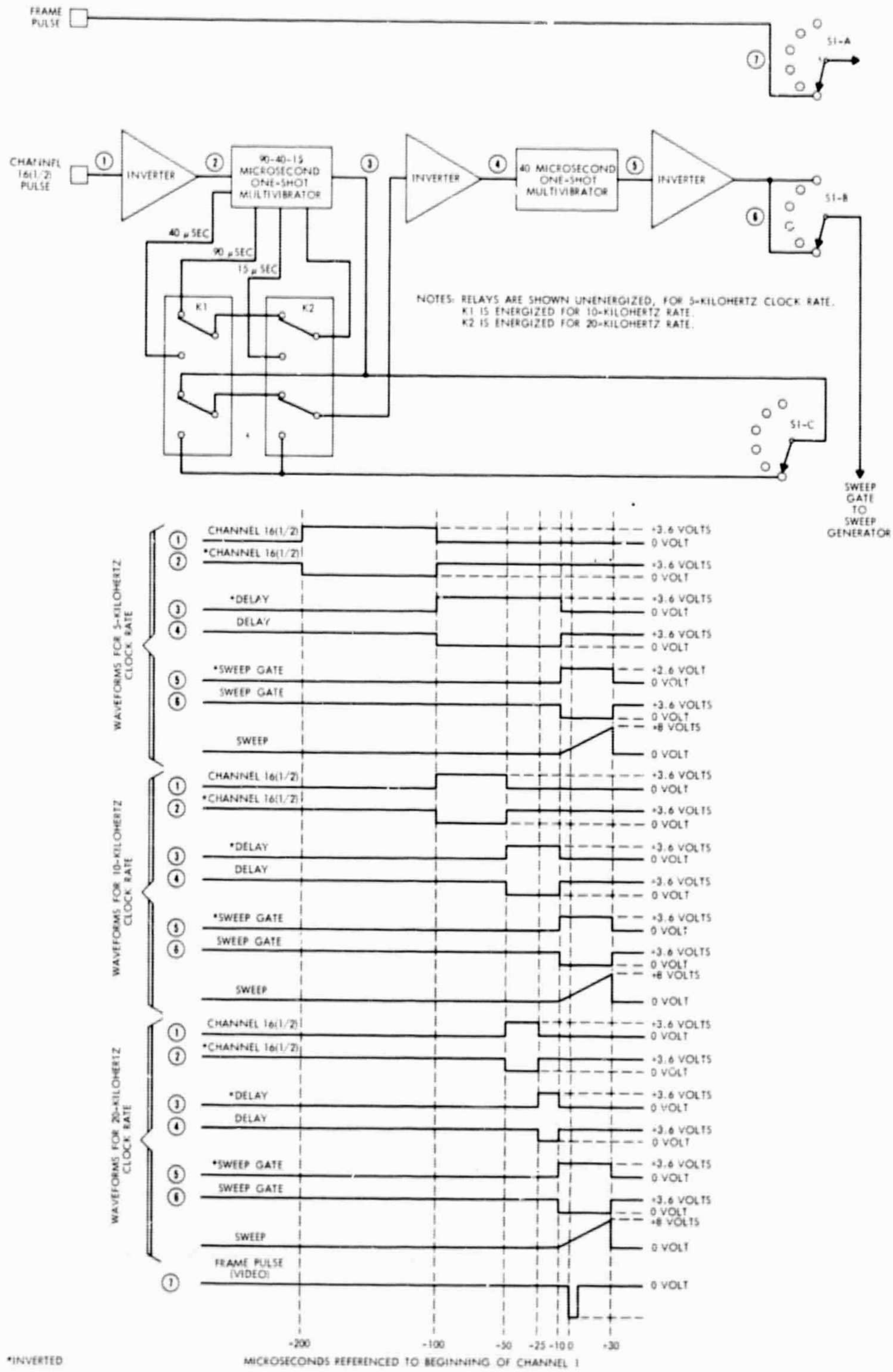


Figure 8. Sweep-Gate Pulse Generation, Diagram and Waveforms for Frame Pulse Display

BUFFER-FEEDBACK CIRCUITRY. Buffering of the sawtooth voltage output of the sweep generator is provided by two transistors connected together in a Darlington-pair emitter follower configuration. This circuit, whose input transistor base is connected across the charging capacitor, presents a high impedance to the resistor capacitor (RC) network, and has an output impedance which is much lower.

A very effective form of feedback is provided by a configuration sometimes known as the bootstrap sweep circuit. A blocking diode is inserted between the +7.5-volt power source and the RC circuit. The output of the Darlington-pair emitter follower circuit is capacitively coupled to the RC network side of the diode. The voltage variations from the emitter follower circuit (essentially, the same as the voltage across the capacitor of the RC network) are superimposed on the +7.5 volts. This causes the voltage across the resistor of the RC circuit to be constant, regardless of the voltage across the capacitor. Therefore, the current through the resistor will be practically constant over the time of the voltage rise, and the voltage across the capacitor will be very nearly linear during this time. Without the feedback which has been explained, the voltage rise is actually exponential, rather than linear. The reason is that, as the voltage across the capacitor increases, the voltage across the resistor decreases, causing a reduced charging rate.

There is another feedback path from the output of the emitter follower to the junction of two capacitors in series which further improves the linearity of the sweep generator output. This pair of capacitors in series are used instead of the one capacitor mentioned in the explanation.

SWEEP-GATE GENERATION. There are three different timing and SWEEP GATE length requirements. Some make use of wave shapes generated by the Servo Clock, and some use, at least, in part, pulses generated within the Video Monitor itself.

SIXTEEN-CHANNEL DATA AND FORMAT. When the source selector switch is in the RECEIVER, 16-CHANNEL DATA position, the output of the receiver is switched to the vertical amplifier, and the sweep is long enough to display all sixteen channels, except for the initial 15 microseconds of Channel 1. In the Servo Clock FORMAT position, the same sweep is used with the vertical circuits connected to the output of the Servo Clock.

The FRAME Pulse is inverted and used to trigger a 15-microsecond one-shot multivibrator. The output of the multivibrator is a +3.6-volt 15-microsecond pulse, repeating itself at 3200-microsecond intervals when the system is operating

at a 5-kilohertz clock rate. This time is cut in half for 10-kilohertz operation, and cut in half again for 20-kilohertz operation. When the selector switch is in either the receiver 16 Channel Video position or in the Servo Clock format position, the 15-microsecond pulse is applied to the base of the discharge transistor of the sweep generator. During the time of the 15-microsecond HIGH pulse, the capacitor is discharged through the transistor; during the zero volt part of the waveform, the capacitor is charged through the resistor. The proper resistor has been selected by the switch and the relays to give a sweep amplitude of 8 volts across the capacitor during the charging time.

CHANNEL-TWO DATA, DISPLAY. When the source selector switch is in either of the two CHANNEL-2 DATA positions (RECEIVER or SERVO CLOCK), the base of the discharge transistor is connected to the inverted CHANNEL-2 pulse. This pulse is a 3.6-volt negative pulse referenced to +3.6 volts. During the time of Channel 2, the transistor base is at zero volts, the transistor is cut off, and the capacitor is being charged. The proper resistor relay chain is connected by the selector switch, and the relays select the correct resistor accoring to the clock rate in use.

RECEIVER, TRIPLE-PULSE DISPLAY. When the system is operating at a 5-kilohertz clock rate, the TRIPLE PULSE begins at the same time as the beginning of Channel 1; but for a 10-kilohertz or 20-kilohertz Clock rate, the TRIPLE PULSE begins 25 microseconds after the start of Channel 1. The sweep length or duration is 40 microseconds in either case. A 40-microsecond 3.6-volt, positive pulse from the 40-microsecond one-shot multivibrator is inverted and applied to the base of the discharge transistor, cutting it off, and allowing the capacitor to be charged.

When the system is operating at a 5-kilohertz clock rate, the 40-microsecond one-shot multivibrator is triggered by a 90-microsecond one-shot multivibrator, which is triggered by the CHANNEL-16 (one-half) pulse input to the Video Monitor. The simplified block diagram and waveform diagram are shown in Figure 6.

For operation at a 10- or a 20-kilohertz clock rate, the 40-microsecond pulse generator is triggered by the trailing edge of an inverted 15-microsecond pulse, the output of a one-shot multivibrator. This multivibrator is triggered by the leading edge of the inverted FRAME pulse input to the Video Monitor. The simplified block diagram and waveforms are shown in Figure 7.

SERVO CLOCK, FRAME DISPLAY. When the selector switch is in the FRAME position, the FRAME output of the Servo Clock is connected to the vertical

amplifiers, to be displayed on the monitor screen. Figure 8 is a simplified diagram of the circuit arrangement necessary to provide the proper sweep for observing this pulse. The CHANNEL-16 (half) pulse, from the Servo Clock, triggers a delay one-shot multivibrator, which in turn, triggers the 40-microsecond one-shot multivibrator. The pulse width of the delay multivibrator is changed by the clock-rate changing relays, giving pulse widths, of 90, 40, and 15 microseconds, for the 5-, 10-, and 20-kilohertz clock rates, respectively. The 40-microsecond multivibrator's output pulse (and, therefore, the monitor sweep) begins 10 microseconds before the FRAME pulse.

DEFLECTION AMPLIFIERS

The video signal, the signal being monitored, is fed into the vertical high-level amplifier circuit, where it is converted to push-pull or double-ended outputs. (See Figures A-1 and A-2 in Appendix.) The two outputs feed the upper and lower vertical-deflection plates of the cathode ray tube, so that the overall transmission characteristics of the system will be symmetrical. Further refinements are, emitter-follower output for power gain, and shunt peaking of the high-level amplifier stage for improved high-frequency response. The horizontal high-level amplifier is quite similar, except that it does not have the high-frequency compensation. The output of the sweep generator is fed into this horizontal amplifier, and its two outputs feed the horizontal plates.

UNBLANKING

Provision has been made so that when no sweep voltage is being applied to the cathode ray tube, its control grid is made sufficiently negative that the electron beam is completely cut off. To cause the trace on the tube to be visible during sweep time, the SWEEP GATE pulse (see the Discharge Circuitry paragraph, page 11) is inverted and amplified. Then, called the UNBLANKING pulse, it is applied to the cathode ray tube control grid. The grid-bias voltage is adjusted by means of the INTENSITY control (a part of the basic oscilloscope), to such a value that the trace has the desired intensity during sweep time.

DETAILED CIRCUIT DESCRIPTION

All of the active circuitry contained in the Video Monitor plug-in unit is packaged on two printed-wiring cards. The high-level amplifiers, both vertical and horizontal, are contained on the High Voltage amplifier card; the remaining circuitry is on Video Monitor Card Number 1. Appendix-Figures A-1 through A-6 supplement and illustrate the descriptions given in this section.

There is only one type of integrated circuit used; namely, the Fairchild type 91429 Micrologic, a dual two-input gate. Each gate is made up of two transistors with the two emitters connected. The collectors use one common load resistor. With each base used as a separate input, each gate can be used as a negative NAND gate, or a positive NOR gate. If one input is connected to the common emitter point, the circuit becomes a NOT circuit, or inverter amplifier. If one input of each gate is connected to the output of the other, the resulting circuit is a flip-flop. If one of the two connections is made by a capacitor, and the input is returned to ground through a resistor, the circuit becomes a one-shot multivibrator. The duration of its unstable state is determined by the product of the capacitance times the resistance of the two added components.

SOURCE-SELECTOR SWITCH

One wafer of a four-pole six-position wafer switch selects one of the three video signals to be observed: RECEIVER FORMAT, 16-CHANNEL DATA, or the FRAME output from the Servo Clock. Two other wafers select timing pulses to allow the viewing of the whole, or of selected parts of the waveform. This is done by so connecting selected circuits as to generate a SWEEP GATE which begins at the right time, and which has a time duration compatible with the duration of the waveform to be observed. The fourth wafer is part of the sweep-generator circuit. It inserts a timing resistor which will enable the generated sawtooth pulse to reach an 8-volt peak during the SWEEP GATE time. (See Figure A-1.)

RELAYS

Two relays, K1 and K2, operated by externally switched voltages, switch the components, where necessary, for correct operation of the monitor at the different clock rates. Detailed information will be found in the descriptions of the individual circuits. (Figures A-1 and A-3.)

SWEEP GENERATOR

The sweep generator used in the Video Monitor is composed of a capacitor network, a switch-relay-resistor chain, a buffer amplifier, and feedback circuitry. (See Figures 5, A-1 and A-3.) The reference designations in the text refer to Figure A-3.

CAPACITOR NETWORK. The capacitor network replaced the usual single capacitor found in a sawtooth generator. This network is composed of a series pair of capacitors, C12 and C13, connected in parallel with capacitor C11, with one end of the network going to ground. The purpose of connecting two capacitors in series is to provide a point to which to apply feedback.

SWITCH-RELAY-RESISTOR CHAIN. A switch-relay-resistor chain is used instead of the usual single resistor. (See Figures 5 and A-3.) It connects the capacitor network to the positive voltage supply, and it selects a current rate which will cause the capacitor network to be charged to approximately 8 volts during the SWEEP GATE time. The resistors involved are R12 through R18, R28, and R29.

DISCHARGE TRANSISTOR. Discharge transistor Q1 is in parallel with the capacitor network (Figure 5). When the base voltage of transistor Q1 is at zero volt, the transistor does not conduct, and the current through the resistor is allowed to charge the capacitor network. When the base is at +3.6 volts, transistor Q1 has a low enough impedance that the capacitors discharge through it in a very short time.

BUFFER AMPLIFIER. The buffer amplifier is composed of transistors Q2 and Q3, and associated circuitry (Figure 5). The transistors are connected as a Darlington-pair emitter follower. The emitter of transistor Q3 is connected to -10 volts through load resistor R20. The base of transistor Q2 is connected to the junction of the resistor network and the capacitor network of the sweep generator. The collectors of both transistors are connected to the -7.5-volt power supply.

FEEDBACK CIRCUITRY. The resistor-relay-switch network of the sweep generator is connected to the +7.5-volt power supply through blocking-diode CR4 (Figure 5). Capacitor C15 connects the output side of diode CR4 to the emitter of transistor Q3. By means of this feedback path, a sawtooth-shaped voltage is

superimposed on the +7.5-volt power supply. Its negative peaks are clamped at +7.5 volts by diode CR4. This voltage, which is the alternating component of the output of transistor Q3, is a slightly attenuated version of the output of the sawtooth generator, because the gain of the buffer amplifier is slightly less than unity. Therefore, the output voltage of this quasi-power supply is always approximately 7.5 volts higher than the voltage at the output of the sawtooth generator, and the voltage across the resistor is very nearly constant. The charging rate is almost constant, and the sawtooth-voltage rise is practically linear. Another feedback path has been provided from the emitter of transistor Q3, through resistor R19, to the junction of capacitors C12 and C13.

SWEEP-GATE-PULSE GENERATOR AND DELAY CIRCUITRY

The SWEEP-GATE pulse is a 3.6-volt negative pulse, referenced to +3.6 volts (Figures 5 through 8). The pulse is applied to the base of discharge transistor Q1. It turns the transistor off, and allows the resistor-capacitor circuit to be charged during the time of the pulse. The circuits next described are connected, as required, to generate a SWEEP-GATE pulse at the correct time, and of the correct duration.

CHANNEL-TWO PULSE INVERTER. The first gate which uses terminals 1 and 2 as inputs of integrated circuit IC 5, will be designated as gate IC 5a. This gate is changed to an inverter by connecting one of its inputs to ground. It inverts the incoming CHANNEL-2 pulse, and, when the selector switch is in either of the CHANNEL 2 DATA positions, the pulse is applied to the base of transistor Q1, thus becoming the CHANNEL-2 DATA SWEEP-GATE pulse input to the sweep generator.

FRAME-PULSE INVERTER AND FIFTEEN-MICROSECOND PULSE GENERATOR. The FRAME pulse comes in as a 4-microsecond -10-volt pulse. (See Figures A-1 and A-3.) It is attenuated and shifted in level, so that the negative peaks of the pulses are clamped at ground potential. The circuit that does this is composed of resistors R1 and R2, and diode CR1. Inverter IC 1a inverts the pulse, and its trailing edge triggers the 15-microsecond pulse generator, IC 2, with its associated circuitry. The output of the pulse generator becomes the SWEEP GATE for the 16-CHANNEL DATA, or FORMAT, displays when the selector switch is set to either of those positions. The SWEEP GATE pulse is that part of the wave in which the voltage is low, or zero volts. For example, when operation is at a 5-kilohertz clock rate, the SWEEP GATE length is 3200 minus 15, or 3185 microseconds. The capacitor network is discharged during the 15-microsecond 3.6 voltage positive pulse.

FORTY MICROSECOND PULSE GENERATOR AND TWO INVERTERS. When the selector swtich is in the TRIPLE PULSE position and the station is set for operation at the 10- or 20-kilohertz rate, the output of the 15-microsecond pulse generator is connected to inverter IC 3a by means of a set of contacts on whichever relay is energized. Its output triggers the 40-microsecond one-shot multivibrator, whose output is inverted by inverter IC 3b. The resulting 40-microsecond 3.6 volt negative pulse is the SWEEP GATE for the TRIPLE PULSE display at the two higher clock rates. The block diagram and waveforms for this setting are shown in Figure 7. Also see Figures A-1 and A-2, in the Appendix.

TRIPLE-WIDTH PULSE GENERATOR. Integrated circuit IC 6, with its associated circuitry, form a one-shot multivibrator which can produce an output pulse of any one of three different widths or durations. The pulse duration is a function of the timing capacitor used.

This one-shot multivibrator has three timing capacitors, only one of which can be connected to the multivibrator at a time. The switching of the capacitors is accomplished by contacts on the Clock-rate-changing relays K1 and K2. A 90-microsecond pulse is generated when operation is at a 5-kilohertz clock rate. The pulse duration is 40 microseconds, at a 10-kilohertz clock rate, and a 15-microsecond pulse is produced at the 20-kilohertz rate. When the source-selector switch is in the TRIPLE PULSE position, but neither relay K1 or K2 is energized, the 90-microsecond output of the triple-width pulse generator is connected to inverter IC 3a through a set of contacts on relays K1 and K2, in series. The output of inverter IC 3a triggers the 40-microsecond pulse generator, whose output, when inverted, is the SWEEP-GATE pulse for the TRIPLE-PULSE sweep. Figure 6 is a simplified block diagram, and waveform diagram, for this mode of operation. Appendix Figures A-1 and A-3 may be used for reference.

The triple-width pulse generator is triggered by the CHANNEL 16 (half) pulse, after the latter has been inverted by inverter IC 5a. The 90-microsecond output of the triple-width pulse generator delays the triggering of the 40-microsecond SWEEP GATE pulse until 10 microseconds before the beginning of the TRIPLE pulse.

When the selector switch is in the FRAME position, the CHANNEL 16 (half) pulse feeds inverter IC 1a, which in turn, is connected to the triple-width pulse generator. The triple-width pulse generator is connected, through contacts on switch wafer S1-B, rather than through relay contacts, to the inverter-pulse-generator-inverter chain. Each pulse width has been designed to delay the start of the SWEEP GATE, from the time of the end of the CHANNEL 16 (half) pulse until 10 microseconds before the beginning of the FRAME pulse, at the Clock rate being used. Figure 8 gives the simplified block diagram and waveform diagram. Also, refer to Appendix Figures A-1 and A-3.

VOLTAGE REGULATOR

For the integrated circuits, the 10-volt incoming supply voltage is reduced to 3.6 volts. Transistor Q6, type 2N2043, has its collector connected to the +10 volt supply, and its emitter to the load. The base is connected to the junction of resistors R24 and R25. The series pair of resistors is connected between ground and a zener-diode stabilized voltage source. The resistance value for resistor R24 must be chosen for each card, so that the voltage at the base of transistor Q6 will cause the output of transistor Q6 to be 3.6 volts ±5 percent.

UNBLANKING CIRCUITRY

Transistor Q5, type 2N3643, inverts the SWEEP GATE pulse, and amplifies it to a peak of +10 volts. This pulse, then designated the UNBLANKING pulse, is connected, through pin 28 of Video Monitor Card 1 and a jumper on the high-level amplifier card, to a two-stage resistance-coupled amplifier on the main chassis of the oscilloscope. This addition to the oscilloscope circuitry is shown in Figure A-4. This amplifier, composed of two transistors and their associated circuitry, amplify the UNBLANKING pulse to an excess of 40 volts.

A limiting circuit, composed of two zener diodes in series, and returned to ground, clips the UNBLANKING pulses at a 40-volt amplitude. The pulse output is resistance-capacitance coupled to the control grid of the cathode-ray tube. The grid is normally biased below the beam cut-off point for the tube, but during the time of the UNBLANKING pulse, the grid reaches a voltage that will allow the trace to be visible. The bias is adjustable by means of a BRIGHTNESS control on the front panel of the oscilloscope. This control is adjusted, during operation, for the desired brightness of the display.

HIGH LEVEL DEFLECTION AMPLIFIERS

The high-level Amplifier card contains two amplifiers, one for each pair of deflection plates of the cathode-ray tube. These amplifiers raise the 8- to 10-volt sweep and video inputs to levels in the 80- to 100-volt range. Figure A-2, in the Appendix, shows a schematic diagram of this card.

VERTICAL-DEFLECTION AMPLIFIER. The vertical-deflection amplifier is composed of transistors Q2 through Q5, with their associated circuitry. The video signal is brought in, through the VERTICAL-GAIN control, to the base of transistor Q2. Transistor Q2 is used as an emitter follower, and its output drives the base of transistor Q4. Transistors Q3 and Q4 form a self-balancing

phase-inverter-amplifier circuit, giving outputs which are 180 degrees out of phase with one another. Because this high-level amplifier stage has relatively high impedance, it incorporates a method of high-frequency compensation known as shunt peaking. This compensation consists of the addition of the inductor-damping-resistor combinations L1-R3 and L2-R6. An inductance is used which will resonate with the circuit shunt-capacitance, at a frequency somewhat above that at which the gain of an uncompensated amplifier would begin to fall off. The shunt resistor prevents sharp peaks in the response curve.

The stage just described is direct-coupled to a double-ended emitter-follower stage consisting of transistors Q5 and Q6, and emitter load resistors R8 and R9. The emitter-follower stage drives the two horizontal deflection plates of the cathode-ray tube.

The HORIZONTAL-POSITION control is a potentiometer whose two end terminals are connected, one to each emitter of the amplifier phase-inverter stage, and whose center tap is connected to the -10-volt supply. Rotating the control varies the bias on transistors Q3 and Q4 in opposite directions. These variations produce corresponding shifts in d-c levels throughout the amplifier, and cause the trace on the cathode-ray tube to be moved up or down.

HORIZONTAL-DEFLECTION AMPLIFIER. The horizontal-deflection amplifier is similar to the vertical amplifier, except that the high-frequency compensation is not used.

TWENTY-KILOHERTZ PHASE-REFERENCE MARKS

For accuracy of transfer of data, the operator must use great care in setting up the PPM system. The Servo-Clock output must be precisely in phase with the incoming telemetry signal. While an oscillator with automatic frequency control is usually adjusted so that the control voltage, as shown on the front panel meter, reads zero, in the PPM system an alternate method has been found to give a more precise indication. This method consists of connecting an output of the 20-kilohertz counter stage, in the Servo Clock, to one end of the vertical centering control in the Video Monitor. Connected at this point, it gives an indication on the cathode-ray tube screen, consisting of small pulses at 25-microsecond intervals. Every second pulse is positive, and the alternate pulses are negative. When aligning the Servo Clock, set the Video Monitor for "RECEIVER, TRIPLE PULSE," and adjust the Servo Clock so that the leading edge of the first pulse of the TRIPLE PULSE is synchronized with one of the phase-reference markers. For a 5-kilohertz clock rate, align the TRIPLE PULSE with a positive marker pulse. For a 10- or 20-kilohertz rate, align the TRIPLE PULSE with a negative

marker. Figures A-1 and A-5 show the lead that connects the Video Monitor to the 20-kilohertz output terminal of the Servo Clock.

VIDEO MONITOR PLUG-IN UNIT WIRING

Figure A-6 is a diagram of the internal wiring of the Video Monitor plug-in unit.

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APPENDIX A

This section consists of diagrams which support the descriptions of the Video Monitor circuitry and the explanations of the equipment operation.

A block diagram of the Video Monitor Plug-in Unit is shown in Figure A-1, while Figures A-2 and A-3 are schematic diagrams of the High-level Amplifier card and Video Monitor Card 1, respectively.

Modifications to the oscilloscope unblanking circuitry, to adapt the oscilloscope to Video Monitor use, are shown in Figure A-4. Figure A-5 is a diagram showing the revised wiring to the oscilloscope plug-in unit connectors.

Figure A-6 is a diagram of the Video Monitor Plug-in Unit wiring, showing connections from card to card, and from the cards to the external circuitry.

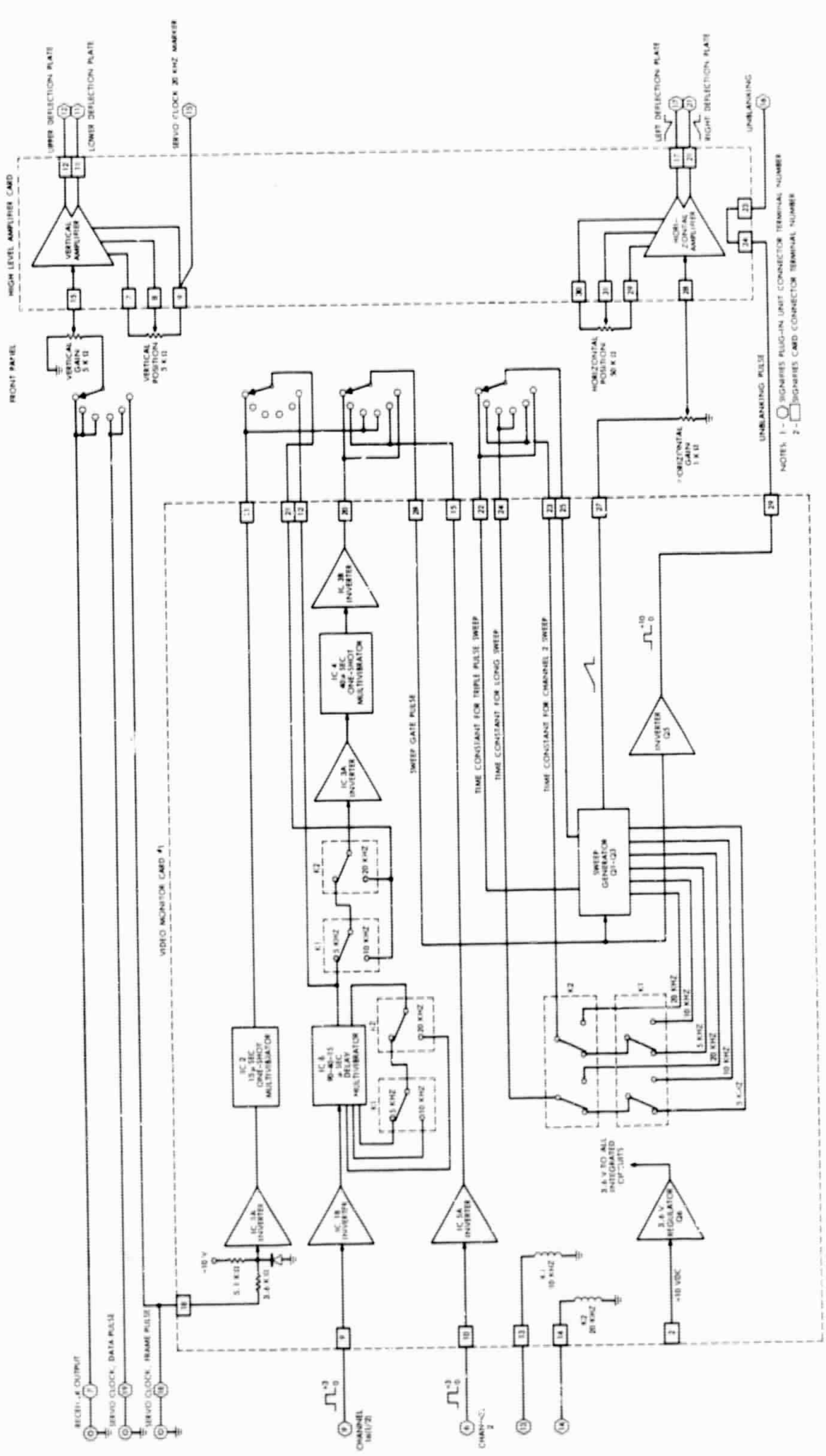
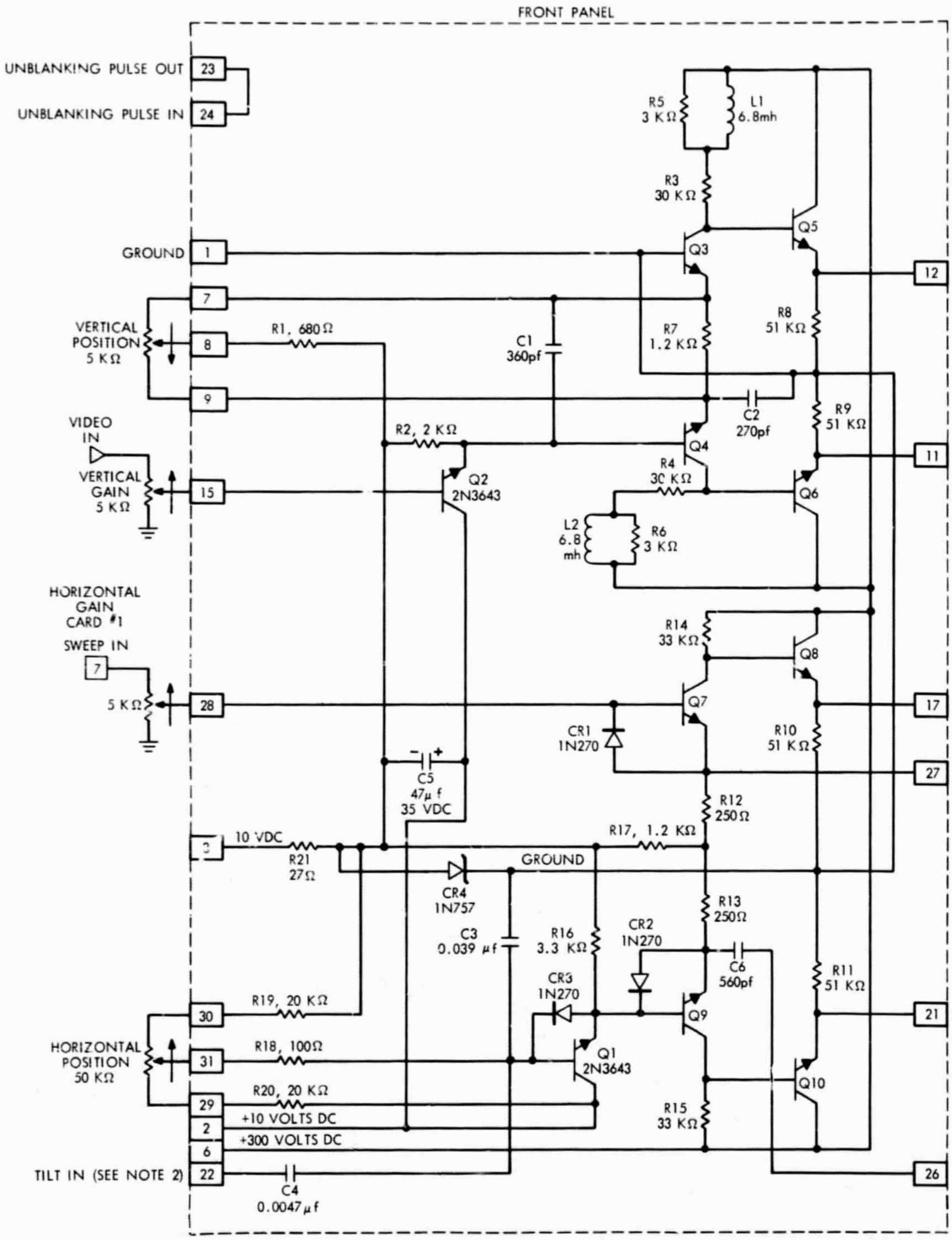
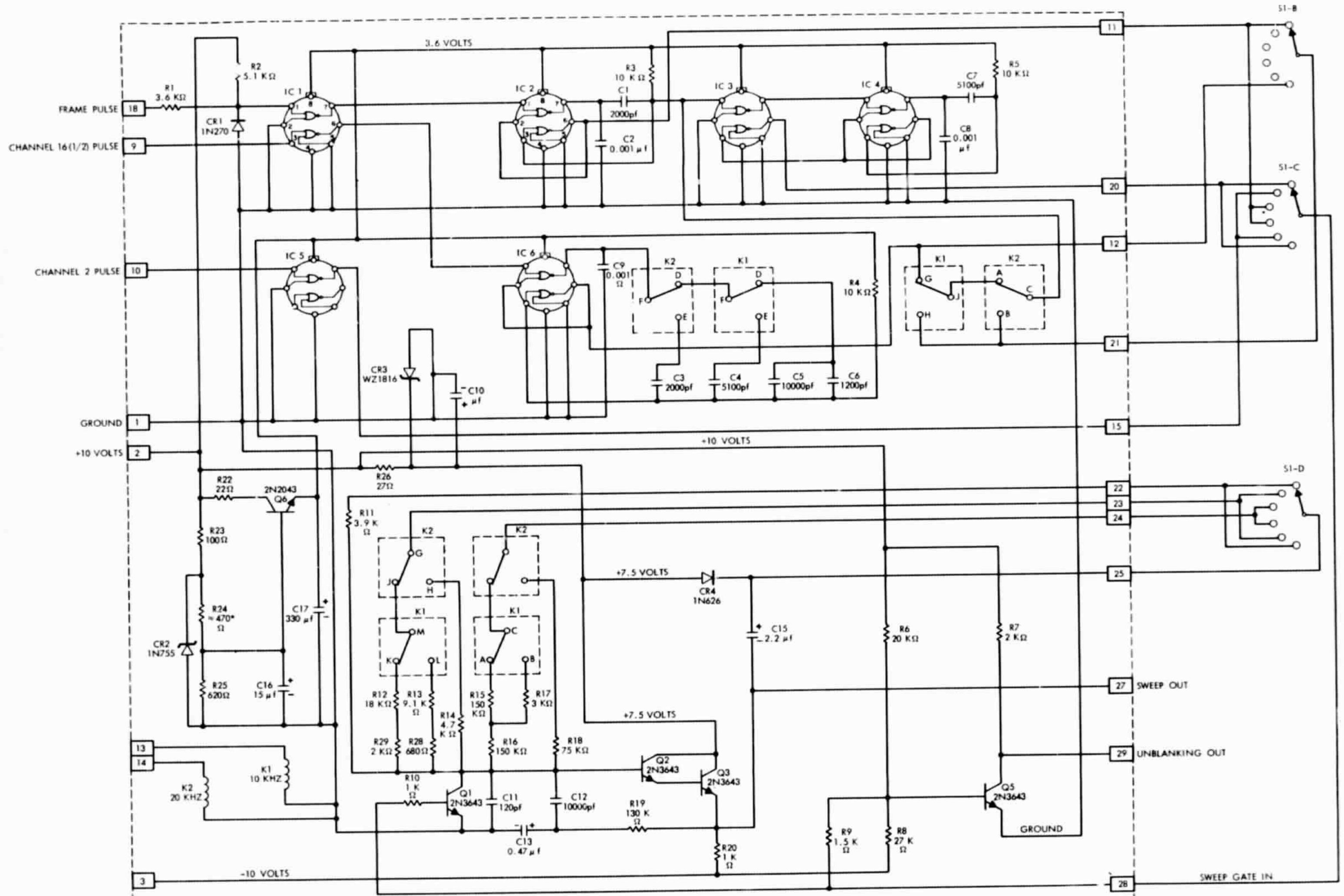


Figure A-1. Video Monitor Plug-In Unit, Block Diagram



NOTES:
1. TRANSISTORS Q3 THRU Q10, ARE TRS 301 LC (INDUSTRO CORP.) WITH THERMALLOY 2210B HEAT SINK.
2. PIN #22 IS NOT USED ON VIDEO MONITOR.

Figure A-2. High-Level Amplifier Card, Schematic Diagram



*R24 TO BE SELECTED TO OBTAIN 3.6 V ± 5% OUTPUT.

RELAYS K1 and K2 ARE SHOWN UNENERGIZED, FOR 5 KILOHERTZ CLOCK RATE.

Figure A-3. Video Monitor, Card 1, Schematic Diagram

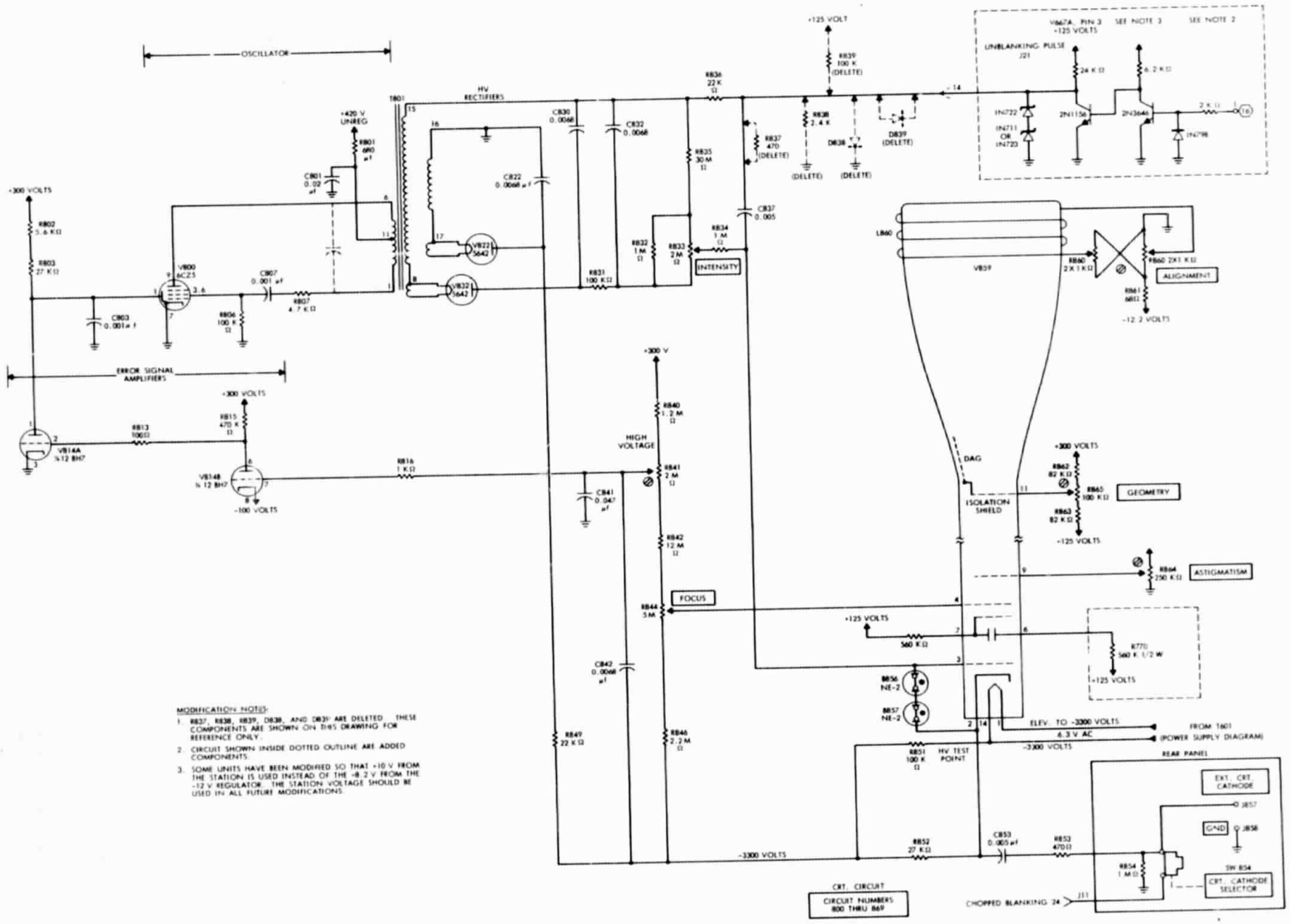


Figure A-4. Video and Bar-Graph Monitors, Modifications to Oscilloscope Unblanking Circuitry, Schematic Diagram

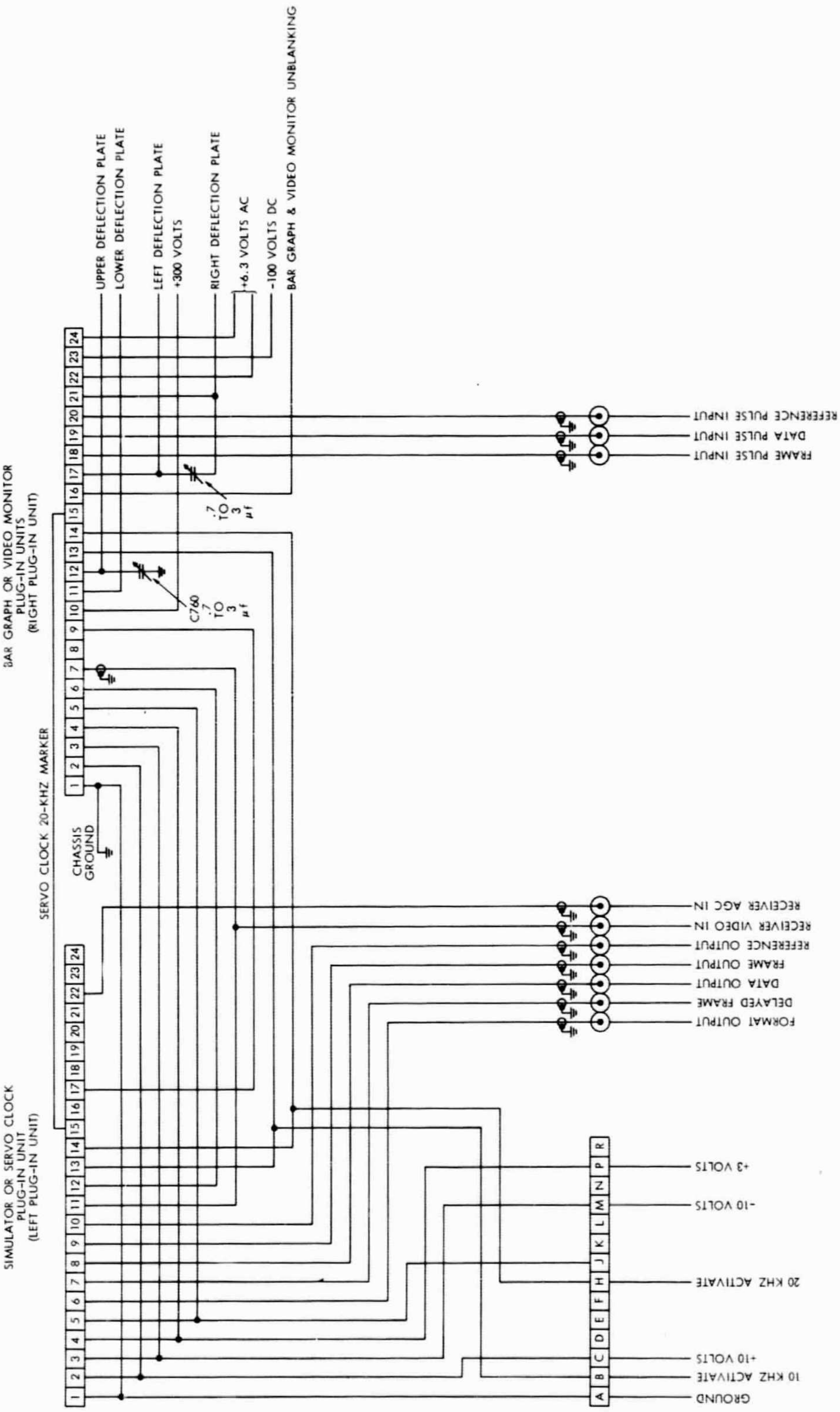


Figure A-5. Oscilloscope, Wiring to Plug-In Unit Connectors

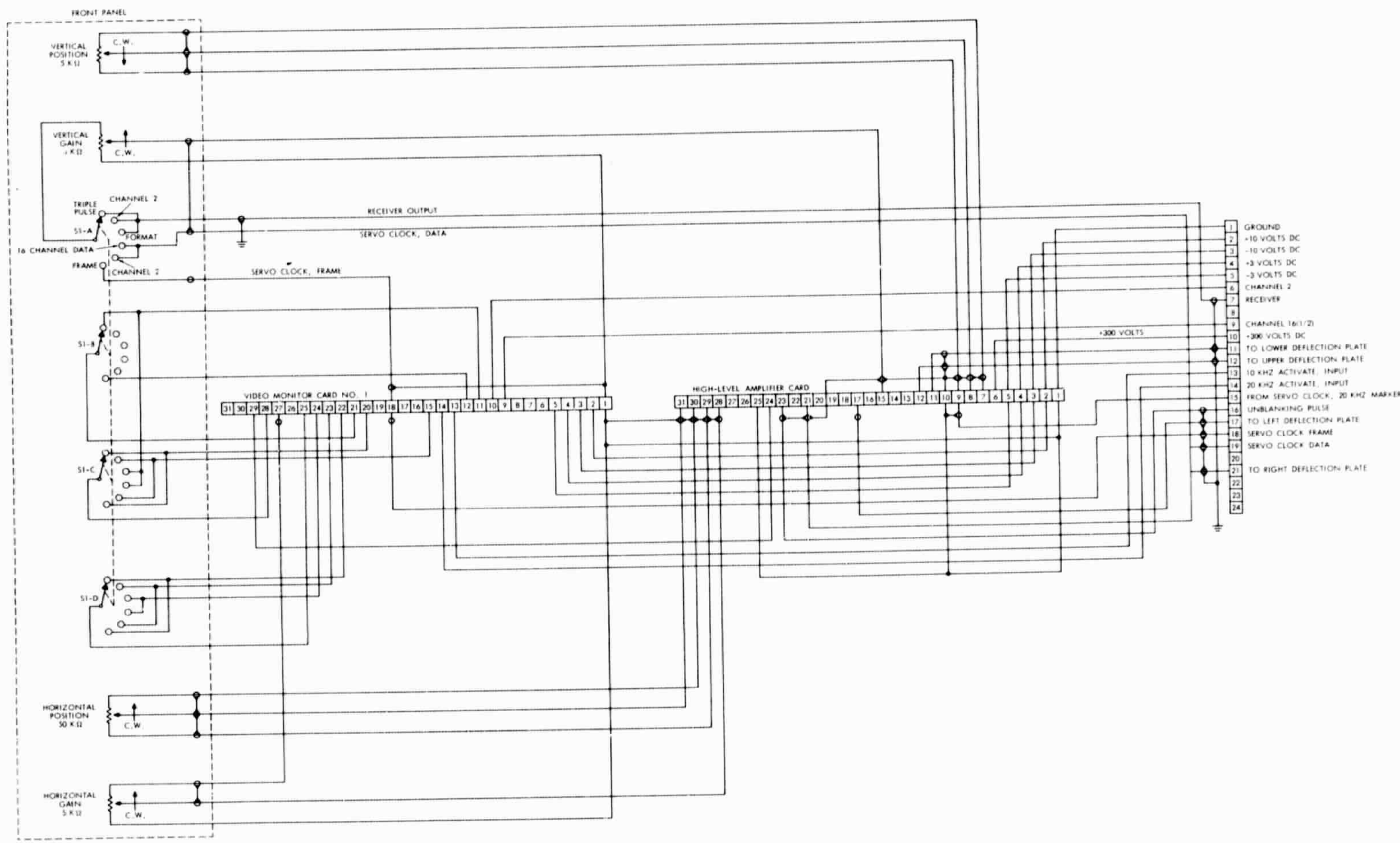


Figure A-6. Video Monitor, Plug-In Unit, Wiring Diagram